Claims:

1. A method of performing video encoding comprising:

adjusting a video encoding rate employed during video encoding based at least in part on a measurement of the variation in pixel values for a selected portion of a video image being encoded and on a bit budget.

2. The method of claim 1, wherein the selected portion of the video image comprises a macroblock.

3. The method of claim 2, wherein the video encoding rate is also adjusted based at least in part on the type of macroblock.

4. The method of claim 3, where in the types comprise at least one of the following: intra, inter, 4 MV, and B.

5. The method of claim 1, wherein the measurement of the variation comprises the sum of absolute differences (SAD).

6. The method of claim 1, wherein the video encoding rate is adjusted by adjusting the quantization step size employed during video encoding.

7. The method of claim 6, wherein the selected portion of the video image comprises a macroblock.

8. The method of claim 7, wherein the video encoding rate is also further adjusted based at least in part on the type of macroblock.

9. The method of claim 8, wherein the types comprise at least one of the following: intra, inter, 4 MV, and B.

10. The method of claim 1, wherein the video encoding performed is substantially MPEG or H.26x compliant.

11. A device having the capability to perform video encoding comprising:

a mechanism to adjust a video encoding rate employed during the video encoding based at least in part on a measurement of the variation in pixel values for a selected portion of a video image being encoded and on a bit budget;

wherein said mechanism is implement within a video encoder.

12. The device of claim 11, wherein said video encoder is implemented in silicon on at least one integrated circuit.

13. The device of claim 12, wherein the silicon implementation of said video encoder comprises microcode.

14. The device of claim 12, wherein the silicon implementation of said video encoder comprises firmware.

15. The device of claim 11, wherein said video encoder is implemented in software capable

of executing on a processor.

16. The device of claim 15, wherein said processor comprises a microprocessor.

17. An article comprising: a storage medium, said medium having stored thereon instructions that, when executed, result in the performance of video encoding by:

adjusting a video encoding rate employed during video encoding based at least in part on a measurement of the variation in pixel values for a selected portion of a video image being encoded and on a bit budget.

18. The article of claim 17, wherein said medium further has stored thereon instructions that, when executed, result in the selected portion of the video image being encoded comprising a macroblock.

19. The article of claim 18, wherein said medium further has stored thereon instructions, that, when executed, result in the video encoding rate being adjusted also based at least in part on the type of macroblock.

20. The article of claim 17, wherein said medium further has stored thereon instructions that, when executed, result in the measurement of the variation comprising the SAD.

21. The article of claim 17, wherein said medium further has stored thereon instructions that, when executed, result in the video encoding rate being adjusted by adjusting the quantization step size employed during video encoding.

22. A video processing platform comprising:

a video encoder;

a video input device coupled to said video encoder; and

memory;

wherein said memory is coupled to said video encoder to store video encoded by said video encoder; and

wherein said video encoder includes a mechanism to adjust a video encoding rate employed during video encoding based at least in part on a measurement of the variation in pixel values for a selected portion of a video image being encoded and on a bit budget.

23. The system of claim 22, wherein the selected portion of the video image comprises a macroblock.

24. The system of claim 23, wherein the mechanism to adjust the video encoding rate employed during video encoding is also based at least in part on the type of macroblock.

25. The system of claim 22, wherein the measurement of the variation comprises the SAD.

26. The system of claim 22, wherein the mechanism to adjust the video encoding rate employed during video encoding is adjusted by adjusting the quantization step size employed during video encoding.

27. A method of performing video decoding comprising:

decoding video that has been encoded, wherein said encoded video was encoded by adjusting a video encoding rate employed during video encoding based at least in part on a

measurement of the variation in pixel values for a selected portion of a video image being encoded and on a bit budget.

28. The method of claim 27, wherein the selected portion of the video image comprises a macroblock.

29. The method of claim 28, wherein the video encoding rate is also adjusted based at least in part on the type of macroblock.

30. The method of claim 27, wherein the measurement of the variation comprises the SAD.

31. The method of claim 27, wherein the video encoding rate is adjusted by adjusting the quantization step size employed during video encoding.

32. The method of claim 31, wherein the selected portion of the video image comprises a macroblock.

33. The method of claim 32, wherein the video encoding rate is also further adjusted based at least in part on the type of macroblock.

34. A video processing platform comprising:

a video decoder;

a video output device coupled to said video decoder; and

memory;

wherein said memory is coupled to said video decoder to store video previously

encoded by a video encoder, wherein said video encoder included a mechanism to adjust a video encoding rate employed during the video encoding based at least in part on a measurement of the variation in pixel values for a selected portion of a video image being encoded and on a bit budgetS.

35. The system of claim 34, wherein the selected portion of the video image comprises a macroblock.

36. The system of claim 34, wherein the mechanism to adjust the video encoding rate employed during video encoding is also based at least in part on the type of macroblock.

37. The system of claim 34, wherein the measurement of the variation comprises the SAD.

38. The system of claim 34, wherein the mechanism to adjust the video encoding rate employed during video encoding is adjusted by adjusting the quantization step size employed during video encoding.

39. An article comprising: a storage medium, said medium having stored thereon instructions that, when executed, result in the performance of video decoding by:

decoding video that has been encoded, wherein said encoded video was encoded by adjusting a video encoding rate employed during video encoding based at least in part on a measurement of the variation in pixel values for a selected portion of a video image being encoded and on a bit budgetS.

40. The article of claim 39, wherein said medium further has stored thereon instructions

that, when executed, result in the selected portion of the video image being encoded comprising a macroblock.

41. The article of claim 40, wherein said medium further has stored thereon instructions, that, when executed, result in the video encoding rate being adjusted also based at least in part on the type of macroblock.

42. The article of claim 39, wherein said medium further has stored thereon instructions that, when executed, result in the measurement of the variation comprising the SAD.

43. The article of claim 39, wherein said medium further has stored thereon instructions that, when executed, result in the video encoding rate being adjusted by adjusting the quantization step size employed during video encoding.

44. An article comprising:

a storage medium having stored thereon a look up table, said table comprising a relationship between the number of bits and variation in pixel signal values of a plurality of video images for a variety of quantization step sizes;

wherein said storage medium further includes instructions stored thereon to employ the look up table and a bit budget to perform video encoding rate control.

45. The article of claim 44, wherein the look up table is employed to perform video encoding rate control when the instructions are executed by a processor.

46. The article of claim 45, wherein the variation in pixel signal values comprises the SAD.